PATENT
Customer No. 22,852
Attorney Docket No. 04329.2306

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Yoshio Ozawa et al.	)	Group Art Unit: 2823
	)	
Application No.: 09/559,757	)	Examiner: Pham, Thanh V.
	)	
Filed: April 27, 2000	)	Confirmation No. 2923
	)	
For: METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE USING AN OXIDATION PROCESS	)	

Attention: Mail Stop Appeal Brief-Patents
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Sir:

APPEAL BRIEF UNDER RULE § 41.37

In support of the Notice of Appeal filed November 5, 2005, further to 37 C.F.R. § 41.37, Appellants present this brief and enclose herewith a check for the fee of $500.00 required under 37 C.F.R. § 41.20(b)(2).

This Appeal is filed to appeal the rejection of claims 8-15, and 20-21 set forth in the final Office Action mailed June 28, 2005.

The period for submitting this brief has been extended through February 6, 2006 (February 5, 2006, being a Sunday), by a Petition for Extension of Time of one month and fee payment filed contemporaneously herewith.

If any additional fees are required or if the enclosed payment is insufficient, Appellants request that the required fees be charged to Deposit Account No. 06-0916.

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I. REAL PARTIES IN INTEREST

The real party in interest is Kabushiki Kaisha Toshiba, a corporation of Japan, the assignee of the entire right, title, and interest in the application.

II. RELATED APPEALS AND INTERFERENCES

There are currently no other appeals or interferences, of which Appellants, Appellants' legal representative, or Assignee are aware, that will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 8-21 are pending in the above-captioned patent application, of which claims 16-19 have been withdrawn from consideration. Claims 8-15, 20, and 21 are under current examination and are the subject of this appeal.

In the June 28, 2005 Office Action, the Examiner rejected claims 8-15, 20, and 21 under 35 U.S.C. § 103(a) as being unpatentable over Applicants' allegedly admitted prior art ("AAPA") in combination with Hisamune (U.S. Patent No. 6,414,352 B1) ("Hisamune"), Aminzadeh, et al. (U.S. Patent No. 6,707,120 B1) ("Aminzadeh"), and Wolf, et al. ("Silicon Processing for the VLSI Era," v.1, 1986, pp. 161-238) ("Wolf"), for the reasons set forth in the June 28, 2005, Office Action.

The claims on appeal are set forth in Section IX entitled "Claims Appendix."

IV. STATUS OF AMENDMENTS

Appellants filed an Amendment on May 11, 2005, which has been entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention, as recited in claim 8, is directed to a method of manufacturing a semiconductor device (*See* Figs. 1A-1F and page 21, line 26 – page 22, line 2) comprising the step of forming an insulating film containing silicon and nitrogen on a semiconductor substrate (*See* page 22, lines 3-11, "a silicon oxide film [is] formed on a flattened surface of the silicon substrate 1. Then, ... nitrogen is introduced into the portion of the silicon oxide film .... Thus, a silicon oxinitride film 2 serving as the gate insulating film is formed.") The method further comprises forming a film (*See* polycrystalline film 3 in Fig. 1C and page 22, lines17-19) which must be processed (*See* Fig. 1D and page 23, lines 8-11, "the polycrystalline silicon film 3 [is etched] by performing dry etching so that the gate electrode 3 is formed") and which contains silicon on the insulating film (*See* page 22, lines 12-15, "[a] polycrystalline silicon film having a thickness of 150 nm [is formed] on the silicon oxinitride film 2"). In addition, the method includes processing the film which must be processed to cause a portion of the insulating film to be exposed to the outside (*See* Fig. 1D showing a portion of silicon oxinitride film 2 to the left of gate electrode 3 being exposed, see also page 23, lines 19-21.) The method further includes lowering a surface of the semiconductor substrate under a part of the insulating film relative to a surface of the semiconductor substrate under the film which is processed to cause the portion of the insulating film to be exposed to the outside (*See* Fig. 2A (an enlarged view of gate 3 and oxinitride film 2), which illustrates a portion of the substrate 1 beneath post oxidation film 5 (i.e., oxinitride film 2 after oxidation in an atmosphere of ozone and oxygen, Fig. 1E and page 23, lines 15-25) being lower than a portion of oxinitride film 2 beneath gate electrode 3). Such lowering is through application of thermal oxidation to a semiconductor structure obtained owing to the above steps (*See* Figs. 1A-1D). The thermal oxidation uses an oxidizing gas containing

one of ozone and oxygen radicals (*See* Fig. 1E, page 25, lines 21-25, "the heat treatment is performed in the ozone atmosphere to perform the post oxidation. A similar effect can be obtained when the heat treatment is performed in an oxygen radicals atmosphere"), and the oxygen radicals are generated by a remote plasma oxidizing method (*See* page 29, lines 20-24, "the silicon substrate is introduced into a remote plasma oxidizing furnace") or by reacting a first gas containing oxygen and a second gas containing hydrogen (*See* page 35, lines 15-19, "while introducing mixed gas of oxygen and hydrogen (oxygen is 50%) into the furnace, heat treatment [of silicon substrate 1] is performed at 900°C, for 10 seconds at 650 Pa.") The method also requires a concentration of nitrogen of the part of the insulating film under an edge portion of the film being decreased by the thermal oxidation process (*See* Fig. 2A in which a portion of oxinitride film 2 marked with diagonal lines has a high nitrogen concentration, but an upper portion of oxinitride film 2 adjacent gate electrode 3, lacking such diagonal lines, has a lower nitrogen concentration. See also page 25, lines 7-10, "[the] nitrogen adjacent to the lower edge of gate electrode 3 ... is dissociated.")

The invention as recited in claim 12 is directed to a method of manufacturing a semiconductor device (*See* Figs. 1A-1F and page 21, line 26 – page 22, line 2) comprising the step of forming an insulating film containing silicon and nitrogen on a semiconductor substrate (*See* page 22, lines 3-11, "a silicon oxide film [is] formed on a flattened surface of the silicon substrate 1. Then, ... nitrogen is introduced into the portion of the silicon oxide film .... Thus, a silicon oxinitride film 2 serving as the gate insulating film is formed.") The method further comprises forming a film (*See* polycrystalline film 3 in Fig. 1C and page 22, lines17-19) which must be processed (*See* Fig. 1D and page 23, lines 8-11, "the polycrystalline silicon film 3 [is etched] by performing dry etching so that the gate electrode 3 is formed") and which contains

silicon on the insulating film (*See* page 22, lines 12-15, "[a] polycrystalline silicon film having a thickness of 150 nm [is formed] on the silicon oxinitride film 2"). In addition, the method includes processing the film which must be processed to cause a portion of the insulating film to be exposed to the outside (*See* Fig. 1D showing a portion of silicon oxinitride film 2 to the left of gate electrode 3 being exposed, see also page 23, lines 19-21.) The method further includes lowering a surface of the semiconductor substrate under a part of the insulating film relative to a surface of the semiconductor substrate under the film which is processed to cause the portion of the insulating film to be exposed to the outside (*See* Fig. 2A (an enlarged view of gate 3 and oxinitride film 2), which illustrates a portion of the substrate 1 beneath post oxidation film 5 (i.e., oxinitride film 2 after oxidation in an atmosphere of ozone and oxygen, Fig. 1E and page 23, lines 15-25) being lower than a portion of oxinitride film 2 beneath gate electrode 3). Such lowering is through application of thermal oxidation to a semiconductor structure obtained owing to the above steps (*See* Figs. 1A-1D). The thermal oxidation uses an oxidizing gas containing one of ozone and oxygen radicals (*See* Fig. 1E, page 25, lines 21-25, "the heat treatment is performed in the ozone atmosphere to perform the post oxidation. A similar effect can be obtained when the heat treatment is performed in an oxygen radicals atmosphere"), and the oxygen radicals are generated by a remote plasma oxidizing method (*See* page 29, lines 20-24, "the silicon substrate is introduced into a remote plasma oxidizing furnace") or by reacting a first gas containing oxygen and a second gas containing hydrogen (*See* page 35, lines 15-19, "while introducing mixed gas of oxygen and hydrogen (oxygen is 50%) into the furnace, heat treatment [of silicon substrate 1] is performed at 900°C, for 10 seconds at 650 Pa.") The method also requires a concentration of nitrogen of the part of the insulating film under an edge portion of the film being decreased by the thermal oxidation process (*See* Fig. 2A in which a portion of

oxinitride film 2 marked with diagonal lines has a high nitrogen concentration, but an upper portion of oxinitride film 2 adjacent gate electrode 3, lacking such diagonal lines, has a lower nitrogen concentration. See also page 25, lines 7-10, "[the] nitrogen adjacent to the lower edge of gate electrode 3 ... is dissociated.") The method additionally includes a step of subjecting the semiconductor structure subjected to the oxidation process to at least one of a nitridation process (*See* page 26, lines 15-18, "a usual nitrogen introducing process is added which is, for example, heat treatment which is performed in a nitrogen gas atmosphere such as nitrogen monoxide after the post oxidation") and an additional oxidation process (*See* page 25, line 25 – page 26, line 2, "[w]hen the thickness of the post oxidation film obtained by performing the post oxidation by using ozone or the oxygen radicals is insufficiently small, usual oxidation is additionally performed after the post oxidation.")

VI. GROUNDS OF REJECTION TO BE REVIEWED

1. Claims 8-15, 20, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in combination with Hisamune, Aminzadeh, and Wolf.

VII. ARGUMENT

1. The rejection of claims 8-15, 20, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in combination with Hisamune, Aminzadeh, and Wolf should be reversed.

In order to properly maintain the rejection under Section 103(a), "the prior art reference (or references when combined) must teach or suggest all the claim limitations." *See* M.P.E.P. §§ 2142, 2143, and 2143.03. Since establishing a *prima facie* case of obviousness requires that the cited reference or references teach or suggest each and every element of the claimed invention, the Examiner's 35 U.S.C. § 103(a) rejection fails on at least this point. In particular, the Examiner has at least failed to show that any of the applied references teach or suggest the claimed "lowering a surface of the semiconductor substrate under a part of the insulating film [containing silicon and nitrogen]" and a "concentration of nitrogen of the part of the insulating film under an edge portion of the film being decreased by the thermal oxidation process," as recited in each of independent claims 8 and 12.

At the outset, and by way of background, in manufacturing semiconductor devices, a silicon substrate may be subjected to oxidation in an atmosphere containing molecular oxygen (O_2) or water to form a relatively thick oxide layer. The thick oxide consumes silicon below the surface of the substrate so that the substrate surface beneath the thick oxide is, in effect, lowered. The thick oxide layer, however, does not form over those portions that are not exposed to the molecular oxygen. As a result, the oxide narrows in a direction toward the covered portion of the substrate to yield a so-called "bird's beak" structure.

Turning to the teachings applied in the final Office Action, the Examiner asserts that "applicant's admitted prior art teaches 'bird's beak oxidation owing to the post oxidation (the

instant specification, page 20's last line)." Final Office Action at page 3. While Figs. 15A to 15C show a silicon oxinitride film 95, the substrate surface beneath film 95 in each of these figures is *flat* and does not include any lowered portions. Indeed, the cited portion of Applicants' specification, in its entirety, reads "[t]he silicon oxinitride file 95 present on the silicon subsequent 91 prevents supply of the oxidizer to the surface of the silicon substrate 91. *Therefore*, bird's beak oxidation owing to the post oxidation *becomes insufficient.*" Emphasis added. Specification at page 20, line 24 - page 21, line 1. Thus, contrary to the Examiner's assertions, AAPA does not suggest bird's beak formation, and thus certainly fails to teach the claimed step of "*lowering* a surface of the semiconductor substrate *under a part of the insulating film* [containing silicon and nitrogen]" (emphasis added), as recited in claims 8 and 12.

The Examiner further asserts that Hisamune teaches an oxidation process in which oxygen radicals are created and in which a "gate bird's beak" is formed. Final Office Action at pages 3 and 4, citing col. 2, lines 64 to col. 3, line 7 of Hisamune. The cited portion of Hisamune, however, is silent as to an insulating film including silicon and nitrogen, and thus certainly fails to teach or suggest the claimed step of "lowering a surface of the semiconductor substrate *under a part of the insulating film* [containing silicon and nitrogen]" (emphasis added), as recited in claims 8 and 12.

The Examiner apparently acknowledges that Hisamune teaches the desirabililty of a "bird-beak free ... insulating layer." Final Office Action at page 4. Nevertheless, the Examiner relies on such teachings in alleging that the claimed "lowering a surface of the semiconductor substrate" would have been obvious in view of Hisanume. Id. The cited portion of Hisamune at col. 1, lines 1-9, as well as other portions of the reference (see col. 2, lines 24-28), teach *away*

from bird's beak formation and thus at least fail to teach the claimed "lowering a surface of the semiconductor substrate," as recited in claims 8 and 12.

At pages 8 and 9 of the Final Office Action, the Examiner cites various cases in support of his position that even though Hisamune teaches away from Applicants's claimed invention, the reference is nevertheless properly combinable with AAPA, Aminzadeh and Wolf. Appellants respectfully disagree.

The Examiner first cites In re Susi, 169 USPQ 423 (CCPA) 1971) for the proposition that "disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or *nonpreferred embodiments*" (emphasis added) and Merck and Co. v. Biocraft Laboratories, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989) in asserting that "[a] reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill [in] the art, including *nonpreferred embodiment*" (emphasis added). Hasamune does not describe bird's beak structures as an embodiment of the purported invention described therein. Rather, the thrust of alleged invention in Hasumine is to *avoid* bird's beak entirely. ("This bird's beak causes the amount of ON-current of each memory cell or each peripheral transistor to drop appreciably." Col. 3, lines 8-10; "An object of the present invention [is] to provide a semiconductor device which has eliminated or reduced the bird's beak." Col. 3, lines 24-28).

The Examiner also quotes from Celritas Technologies Ltd. v. Rockwell International Corp., 150 F.3d 1354, 1361, 46 USPQ2d 1516, 1522-23 (Fed. Cir. 1998), for the proposition that "[e]ven a teaching away from a claimed invention does not render the invention patentable." Final Office Action at page 8. In *Celritas*, however, the Court held that even though the prior art taught away from the claimed invention, it can still be *anticipatory*. The Court, however, did *not*

address whether such teachings can be relied upon in the context of obviousness under Section 103. Thus, since claims 8-15, 20, and 21 stand rejected under Section 103, the Examiner's reliance on *Celritas* is misplaced.

The Examiner further relies on *In re Gurley*, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994) in contending that "[a] known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." Final Office Action at page 8. In *In re Gurley*, the claims at issue were directed toward an epoxy based printed circuit material. An applied Yamaguchi reference taught that such epoxy based printed circuit boards were inferior, but acknowledged that they have "relatively acceptable dimensional stability and "some degree of flexibility." Id at 1131. The Court, therefore, found that such teachings rendered Gurley's claims obvious, but, in citing *In re Caldwell,* 319 F.2d 254, 256, 138 USPQ 243, 245 (CCPA 1963), acknowledged that a "reference teaches away if it leaves the impression that the product would not have the property sought by the applicant." Id. at 1132.

Here, Hisamune does not teach or suggest that a bird's beak structure is in any way desirable, or even acceptable for any purpose. Rather, as noted above, according to Hasamune, devices having a bird's beak suffer from an appreciable drop in the "amount of ON-current." Col. 3, lines 8-10. Moreover, Hisamune discloses that "[a]nother problem posed by the bird's beak is to provide a limitation to scaling down of each memory cell." Col. 3, lines 16-17. Clearly, Hisamune describes the bird's beak as an undesirable consequence of oxidation with oxygen radicals. As such, Hisamune teaches away from Applicants' claimed method including "lowering a surface of the semiconductor substrate," as recited in claims 8 and 12.

In addition, Hisamune expressly teaches use of a film including silicon and nitrogen as a *barrier* to oxygen radicals. *See* col. 4, lines 65-67 ("nitride layer 102 has an oxidation proof

property that is effective in preventing oxygen radicals from reaching floating gate 201.") Accordingly, Hisamune teaches a film including silicon and nitrogen to prevent oxidation with oxygen radicals. One of ordinary skill, therefore, certainly would not have turned to Hisamune for teachings of lowering a surface of substrate under an insulating film (containing silicon and nitrogen) through thermal oxidation with an oxidizing gas containing oxygen radicals. Hisamune teaches away from claims 8 and 12 for this additional reason.

The Examiner also contends that the claimed "lowering a surface of the semiconductor substrate" is "inherent as recognized by Aminzadeh et al., figs 2, 6 and the corresponding passages." Final Office Action at page 4. Figs. 2 and 6 of Aminzadeh, however, show substrate 101 (Fig. 2) and substrate 405 (Fig. 6) each having a *flat* surface. No portion of the surface of substrate 101 or substrate 405 is lowered relative to another portion. Moreover, the discussion of Fig. 2 at col. 1, line 56 to col. 2, line 5, and the discussion of Fig. 6 at col. 3, lines 65 to col. 4, line 43 are entirely silent as to any lowering of the substrate surface whatsoever. Appellants fail to see how such teachings disclose, inherently or otherwise, the claimed "lowering a surface of the semiconductor substrate *under a part of the insulating film* [containing silicon and nitrogen]" (emphasis added), as recited in claims 8 and 12.

The Examiner further alleges that:

> [T]he re-oxided nitrided oxide applied on the gate structure of applicant's admitted prior art could increase the thickness of side oxide 201 as pointed out by Aminzadeh et al. (fig. 2 and last line of col. 1 about the prior of Kusunoki et al.) *The same performance as of the instant invention that increases the thickness of side oxide would also make the surface of the obtained semiconductor substrate lower.*
>
> (Emphasis added) Final Office Action at page 9.

Appellants respectfully note that here also the Examiner has merely made an uncorroborated assertion that Aminzadeh teaches a lowered semiconductor substrate surface. As

noted above, there is simply no teaching or suggestion that this is the case: the drawings relied upon in the Final Office Action show a *flat* surface. In addition, Aminzadeh only discloses increasing the thickness of side oxide 201 in a *lateral* direction, *not* in a vertical direction into the substrate to lower the substrate surface. Col. 1, line 66 - col. 2, line 1.

In an effort to further support the alleged inherent teachings of Aminzadeh, the Examiner asserts that "the inherency of 'lowering the surface' is supported by Wolf et al.'s fig. 3, page 202." Final Office Action page 4. The cited portion of Wolf, however, discloses thermal oxidation with either molecular oxygen or water (see Wolf at page 201) of a bare silicon substrate surface (see Fig. 3). No insulative film including nitrogen and silicon is disclosed on the silicon substrate shown in Fig. 3. Accordingly, Wolf cannot teach or suggest, or otherwise evidence inherency of the claimed "lowering a surface of the semiconductor substrate *under a part of the insulating film* [containing silicon and nitrogen]" (emphasis added), as recited in claims 8 and 12.

The Examiner apparently contends that since oxidation of a bare silicon substrate with molecular oxygen or water yields a lowered substrate in Fig. 3 of Wolf, that a lower substrate portion can also be achieved when oxidizing a *different* substrate (i.e., one having a insulative film including nitrogen and silicon) with a *different* oxidizing species, i.e., ozone or oxygen radicals. The Examiner has failed, however, to provide any evidence that the disparate teachings of oxidation at pages 202 and 203 could have been relied upon by one of ordinary skill to predict oxidation using the oxidizing species and substrate recited in claims 8 and 12. Indeed, Wolf clearly teaches that the mathematical model describing oxidation at pages 202 and 203 (Henry's law) "does not hold under conditions of molecular dissociation." *See* Wolf at page 3. Thus, Wolf, on its face, suggests that the teachings of oxidation through exposure to molecular oxygen

or water are inapplicable in describing oxidation with oxygen radicals or ozone, and thus fails to support the Examiner's inherency assertions for this reason also.

Thus, as noted above, neither AAPA, Hisamune, Aminzadeh nor Wolf teaches or suggest the claimed method including "lowering a surface of the semiconductor substrate *under a part of the insulating film* [containing silicon and nitrogen]" (emphasis added), as recited in claims 8 and 12. Claims 8 and 12 are thus distinguishable over the applied references at least for this reason.

The Examiner further contends that "the incorporation of oxidant into the Si/SiO_2, in this case, the insulating film containing silicon and nitrogen, would reduce the concentration of nitrogen of the part of the insulating film under an edge portion of the film by the thermal oxidation process." Final Office Action at page 4. As noted above, there is no teaching in Wolf of an insulating film containing silicon and nitrogen on the substrate shown in Fig. 3 at page 202 of the reference. There is also no teaching of a film containing silicon on such an insulating film. Accordingly, Wolf necessarily fails to teach what the concentration of nitrogen would be in the insulating film in a part of the insulating film under an edge portion of the silicon containing film, *because Wolf fails to teach both the silicon containing film and the insulating film in the first place*. The Examiner has failed to provide any evidence whatsoever to the contrary.

For these additional reasons, claims 8 and 12 are distinguishable over the applied references.

Further, in the "Response to Arguments" section of the Final Office Action, the Examiner first alleged that the "formed structure of applicant's admitted prior art will endure the thermal oxidation of Hisamune to have the semiconductor substrate's surface lowered and the concentration of nitrogen decreased (these symptoms are supported by Wolf)" (Office Action, p. 7). Whether or not the formed structure of AAPA "will endure" Hisamune's thermal oxidation

process does not demonstrate that the cited references teach or suggest the above-quoted claimed combination of process steps *taken as a whole.*

The Examiner alleged that Wolf teaches the claimed thermal oxidation process by virtue of the title of Wolf's chapter 7 being "Thermal Oxidation." "With that point of view, thermal oxidation and CVD process[es] are ways of forming SiO_2" (Final Office Action, p. 8). Again, Applicants note that while Wolf may teach thermal oxidation in Chapter 7, the portions addressed by the Examiner (page 202, cited on page 3 of the Final Office Action) do not lend themselves to combination with Hisamune, Aminzadeh, or AAPA at least because Wolf's discussion of an oxidation model shown in Fig. 3 on p. 202 invokes Henry's law, which "implies that the oxidizing species moves through the oxide *in molecular form, since the law does not hold under conditions of molecular dissociation*" (Wolf, p. 203, emphasis added). As noted above, this contradicts, at least, Appellants' claimed "using an oxidizing gas containing one of *ozone and oxygen radicals*, the oxygen radicals being generated by *remote plasma oxidizing method*" (emphasis added). In addition, Wolf's teaching that "[t]he plasma-enhanced oxide growth process, however, suffers from several disadvantages..." (p. 219), clearly does not provide any motivation to one of ordinary skill in the art to select Wolf in combination with Hisamune to cure the deficiencies of AAPA in relation to the above-quoted elements of independent claims 8 and 12.

Thus, none of the applied teachings, taken alone or in combination, teach or suggest all the elements of independent claims 8 and 12, and therefore this rejection is improper. Appellant has therefore established that AAPA, Hisamune, Aminzadeh, and Wolf taken alone or in combination, do not teach or suggest each and every element of Appellant's independent claims 8 and 12. Accordingly, the Examiner's reliance on AAPA, Hisamune, Aminzadeh, and Wolf

fails to establish *prima facie* obviousness. Dependent claims 9-11, 13-15, 20, and 21 are allowable at least due to their respective dependence from allowable base claims 8 or 12. The improper 35 U.S.C. § 103(a) rejection should be reversed.

For the reasons given above, pending claims 8-15, 20, and 21 are allowable. Appellant respectfully requests that the Board reverse the Examiner's rejection.

To the extent any extension of time under 37 C.F.R. § 1.136 is required to obtain entry of this Appeal Brief, such extension is hereby respectfully requested. If there are any fees due under 37 C.F.R. §§ 1.16 or 1.17 that are not enclosed herewith, including any fees required for an extension of time under 37 C.F.R. § 1.136, please charge such fees to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: February 6, 2006

By: _____
David L. Soltz
Reg. No. 34,731

VIII. CLAIMS APPENDIX

Claims Appendix to Appeal Brief Under Rule 41.37(c)(1)(viii)

8. A method of manufacturing a semiconductor device comprising the steps of:

forming an insulating film containing silicon and nitrogen on a semiconductor substrate;

forming a film which must be processed and which contains silicon on the insulating film;

processing the film which must be processed to cause a portion of the insulating film to be exposed to the outside; and

lowering a surface of the semiconductor substrate under a part of the insulating film relative to a surface of the semiconductor substrate under the film which is processed to cause the portion of the insulating film to be exposed to the outside by applying a thermal oxidation process to a semiconductor structure obtained owing to the above steps, the thermal oxidation process using an oxidizing gas containing one of ozone and oxygen radicals, the oxygen radicals being generated by remote plasma oxidizing method or by reacting a first gas containing oxygen and a second gas containing hydrogen, and a concentration of nitrogen of the part of the insulating film under an edge portion of the film being decreased by the thermal oxidation process.

9. A method of manufacturing a semiconductor device according to claim 8, wherein the insulating film is one of a silicon oxide film containing nitrogen and a silicon nitride film.

10. A method of manufacturing a semiconductor device according to claim 8, wherein the insulating film is a gate insulating film, and the film which must be processed is processed to form a gate electrode.

11. A method of manufacturing a semiconductor device according to claim 8, wherein the insulating film is formed in such a manner that the concentration of nitrogen at an interface of the insulating film with the semiconductor substrate realized before the oxidation process is performed is 5×10^{13} cm^{-2} or higher.

12. A method of manufacturing a semiconductor device comprising the steps of:

forming an insulating film containing silicon and nitrogen on a semiconductor substrate;

forming a film which must be processed and which contains silicon on the insulating film;

processing the film which must be processed to cause a portion of the insulating film to be exposed to the outside;

lowering a surface of the semiconductor substrate under a part of the insulating film relative to a surface of the semiconductor substrate under the film which is processed to cause the portion of the insulating film to be exposed to the outside by applying a thermal oxidation process to a semiconductor structure obtained in the above steps, the thermal oxidation process using an oxidizing gas containing one of ozone and oxygen radicals, the oxygen radicals being generated by remote plasma oxidizing method or by reacting a first gas containing oxygen and

a second gas containing hydrogen, and a concentration of nitrogen of the part of the insulating film under an edge portion of the film being decreased by the thermal oxidation process; and

subjecting the semiconductor structure subjected to the oxidation process to at least one of a nitridation process and an additional oxidation process.

13. A method of manufacturing a semiconductor device according to claim 12, wherein the insulating film is one of a silicon oxide film containing nitrogen and silicon nitride film.

14. A method of manufacturing a semiconductor device according to claim 12, wherein the insulating film is a gate insulating film, and the film which must be processed is processed to form a gate electrode.

15. A method of manufacturing a semiconductor device according to claim 12, wherein the insulating film is formed in such a manner that the concentration of nitrogen at an interface of the insulating film with the semiconductor substrate realized before the oxidation process is performed is not less than 5×10^{13} cm^{-2}.

20. A method of manufacturing a semiconductor device according to claim 8, wherein the thermal oxidation process using the oxygen radicals is performed at not lower than 900°C.

21. A method of manufacturing a semiconductor device according to claim 12, wherein the thermal oxidation process using the oxygen radicals is performed at not lower than 900°C.

IX. EVIDENCE APPENDIX

NONE

X. RELATED PROCEEDINGS APPENDIX

NONE